Kavayitri Bahinabai Chaudhari North Maharashtra University, Jalgaon

'A' Grade NAAC Re-accredited (4th cycle)

Department of Electronics (School of Physical Sciences)

Materials and Devices Laboratory for Nanoelectronics (MDLN)

Class 10K Clean Room

Announces

30 Hrs Hands-on Training Course on "Fabrication of Nano-Scale Semiconductor Devices" in Class 10000 Clean Room [as a Skill Enhancement Course, towards NEP-2020 Implementation]

About Course

The Certificate Course: ***30 Hrs Hands-on Training Course on "Fabrication of Nano-Scale Semiconductor Devices" in Class 10k Clean Room*** is a specialized skill enhancement program designed to provide in-depth knowledge and practical experience in the field of semiconductor technology, with a specific focus on Metal Oxide Semiconductor (MOS) devices fabrication and characterization. The course is typically structured to be completed within 30 hours (2 Credit) in **a week** mostly hands-on training sessions.

Course Contents:

- Introduction and overview of semiconductor device fabrication, MOS Structure, clean room design, classification & Importance.
- Basics of fabrication process: Semiconductor wafer Cleaning (RCA),Oxidation, Doping, Etching, metallization, Annealing etc.
- Introduction to fabrication systems such as PEALD, RTP, Thermal Evaporation etc.
- Characterization Techniques like FTIR, Ellipsometry, Elemental & Electrical Characterization: IV-CV Setup
- Introduction to Lithography: Basics and types of Lithography.

Course Outcome:

- Students will get hands-on training on various nano scale Device Fabrication systems in class **10K Clean Room**
- They will fabricate nano scale devices by their own (prototype) on Si wafer.
- They will get certification of course completion (2 credits) by KBCNMU, Jalgaon

Intended participants:

Engineering & Science Students at UG & PG Level Including Research student having diversified background such as Electronics, E & TC, Instrumentation, Metallurgy, Chemical technology, material science, physics, chemical science etc.

Course Fees Structure and Registration Link

- **Rs 12,000/- per student (*including cost of clean room garment kit and Si wafer, allied chemicals & precursors etc*)**
- **Rs 2,000/- (extra for Accommodation on campus)**
- **Important dates:**

Registration open till : *28/08/2023*

20 Seats only

Confirmation of participation by: *30/08/2023*

Course dates:

Note: *10% Discount in course fees may be given to the group booking of 10 student.*

Registration Link: https://forms.gle/G44GryPrmBAj3w6d7

Organizing Team:

- **Prof. A. M. Mahajan** (Senior Professor and Director, SOPS)
- **Dr. D. J. Shirale** (Assistant Professor)
- **Mr. Vaibhav Borokar** (Researcher)
- **Mr. M. S. Netkar** (Technical Assistant)

For more information contact:

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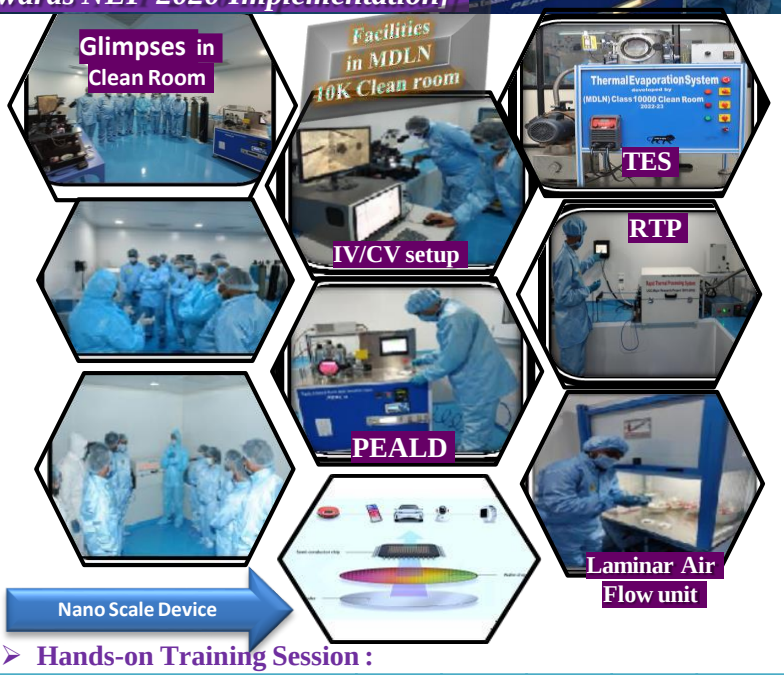

➢ Hands-on Training Session :

Process Details	Day 1	Day 2	Day 3	Day 4	Day 5
Introduction to various Clean room components, protocols, Chemical Treatment Bench (CTB) and familiarization.2 inch Si wafer handling, cleaning (RCA) process by using CTB,	A1	A5	A4	A3	A2
Deposition of High-k (La_2O_3) ultra thin Film on Pre-cleaned silicon substrate by Plasma enhance Atomic Layer Deposition (PEALD) system & Elemental confirmation of deposited high-k film by using FTIR spectroscopy	A2	A1	A5	A4	A3
Post Deposition Annealing (PDA) by Rapid Thermal Annealing on deposited high-k, Metallization (Al) by Thermal Evaporation System and Post Metallization Annealing (PMA) by RTP	A3	A2	A1	A5	A4
Electrical characterization of fabricated Al/La_2O_3/Si MOS Device by using IV/CV setup	A4	A3	A2	A1	A5
Deposition of oxide on Si by sol gel spin on method, Annealing and Introduction of various Lithographic steps	A5	A4	A3	A2	A1

➢ Resource persons for the course :

- **Prof. A. M. Mahajan (Senior Professor & Head, Dept of Electronics)** Having 37 yrs teaching and 20+ years independent research exp in the field of semiconductor technology, having taken exposure of working with **NNIN Nanofab**, UCSB, CA, USA, **MDM Lab**, Agrate Brianza, Itali, **School of Microelectronics (collaboration) Fudan Univ.**, Shanghai & **Dept. of Microelectronics**, **NCUT,** Beijing, China**.** Established well equipped **MDLN research lab (class 10000 clean room)** by the way of obtaining fundings through 10 completed Major research projects and by gaining expertise in handling of fabrication and characterization equipment through 8 completed collaborative projects under **INUP @ CEN, IIT** Mumbai.
- **Dr. D. J. Shirale** (Assistant Professor, Dept of Electronics) **Postdoc @ UCR, CA, USA** having experience of using device fabrication and characterization systems in clean room and research experience of 15+ yrs in the field Nano Sensor Technology

Team of Clean Room System Operators :

- **Prof. A. M. Mahajan** Principal Investigator: MDLN & Class 10k Clean Lab *(Overall Supervision & Monitoring)*
- **Dr. Sumit Patil** (6+ yrs. experience of operating all the systems in MDLN lab &10k clean room)
- **Dr. Viral Barhate** (5+ yrs. experience of operating all the systems in MDLN lab &10k clean room)
- **Vaibhav Borokar** (4+ yrs. experience of operating all the systems in MDLN lab &10k clean room)
- **Bhushan Desale** (1+ yr. experience of PEALD system operation in 10k clean room)
- **Abhishek Chaudhari** (1+ yrs experience of operating Thermal Evaporation and RTP Systems in 10k clean room)